PATENT APPLICATION

THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE HONORABLE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of

Stanton Earl Weaver Jr. et al.

Application No.: 10/582,377

Examiner: H. Jey Tsai

Filed: December 30, 2005

Docket No.: 137295
GLOZ 2 00196 US01

For: SURFACE MOUNT LIGHT EMITTING DIODE CHIP PACKAGE

BRIEF ON APPEAL

Appeal from Group 2895

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I. REAL PARTY IN INTEREST

The real party in interest for this appeal and the present application is GE Lighting Solutions (formerly known as GELcore LLC), by way of an Assignment recorded in the U.S. Patent and Trademark Office at Reel 019172, Frame 0811.

II. RELATED APPEALS AND INTERFERENCES

There are no prior or pending appeals, interferences or judicial proceedings, known to Appellant, Appellant's representative, or the Assignee, that may be related to, or which will directly affect or be directly affected by or have a bearing upon the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-6, 15-31, and 38-41 are on appeal.

Claims 1-31 and 38-41 are pending.

Claims 7-14 are withdrawn.

Claims 1-6, 15-31, and 38-41 are rejected.

Claims 32-37 are canceled.

IV. STATUS OF AMENDMENTS

An Amendment C is being filed concurrently with this Appeal Brief. It is not known whether Amendment C will be entered; however, Appellants expect Amendment C will be entered as it merely deletes an extraneous "the" in claim 21 so as to remove a potential antecedent basis issue, adds a clarifying comma to claim 21, and adjusts the sub-paragraphing of claim 21 to offset the wherein clauses with extra indentation. Nonetheless, the listing of claims in Section VIII does not including these amendments.

A Petition for Withdrawal of Premature Finality of the Office Action Mailed December 28, 2010 was filed January 11, 2011. No decision or other response has yet been received regarding this Petition.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Note: In view of election of the species described with reference to FIGURE 1, only FIGURE 1 and reference numbers appearing in FIGURE 1 are cited here.

The invention of **claim 1** is directed to a light emitting package comprising: a chip carrier (14) having top and bottom principal surfaces (26, 50) (page 3 lines 16-22; page 4 lines 14-15); at least one light emitting chip (12) attached to the top principal surface (26) of the chip carrier (page 3 lines 16-22); and a lead frame (40, 42) attached to the top principal surface (26) of the chip carrier (14) but not to the bottom principal surface (50) of the chip carrier (14) (page 4 lines 7-21).

The invention of **claim 3** is directed to a light emitting package as set forth in claim 1, further comprising one or more areas of electrically conductive material (20, 22) disposed on the top principal surface (26) of the chip carrier (14), the attachment of the lead frame (40, 42) to the top principal surface (26) electrically contacting the one or more areas of electrically conductive material (page 4 lines 8-11).

The invention of **claim 17** is directed to a light emitting package as set forth in claim 1, wherein the lead frame (40, 42) has electrical leads (46, 52) extending from portions of the lead frame attached to the top principal surface (26) of the chip carrier (14), the electrical leads (46, 52) being shaped to include lead portions approximately coplanar with the bottom principal surface (50) of the chip carrier (page 4 lines 12-18).

The invention of **claim 38** is directed to a light emitting package as set forth in claim 1, wherein the lead frame (40, 42) includes electrical leads (46, 52) extending

from portions of the lead frame attached to the top principal surface (26) of the chip carrier (14), the electrical leads (46, 52) being shaped to include lead portions distal from the chip carrier (14) that are approximately coplanar with the bottom principal surface (50) of the chip carrier (page 4 lines 12-18).

The invention of **claim 21** is directed to a light emitting package. A chip carrier (14) has top and bottom principal surfaces (26, 50) (page 3 lines 16-22; page 4 lines 14-15). At least one light emitting chip (12) is attached to the top principal surface (26) of the chip carrier (page 3 lines 16-22). A lead frame (40, 42) is attached to the top principal surface (26) of the chip carrier (page 4 lines 7-12). The lead frame (40, 42) has electrical leads (46, 52) extending from portions of the lead frame attached to the top principal surface (26) of the chip carrier (page 4 lines 12-18). The electrical leads (46, 52) are shaped to include lead portions approximately coplanar with the bottom principal surface (50) of the chip carrier (page 4 lines 12-18). The bottom principal surface (50) of the chip carrier is at least one of substantially electrically non-conductive and electrically isolated from the lead frame (40, 42), and the chip carrier (14), light emitting chip (12), and lead frame (40, 42) define a surface mountable unit (page 4 line 30-page 5 line 1). The light emitting package further includes a printed circuit board (70) on which printed circuitry (80, 82) is disposed (page 5 lines 1-6). The surface mountable unit is mounted on the printed circuitry (80, 82) with the lead portions approximately coplanar with the bottom principal surface (50) of the chip carrier (14) electrically contacting the printed circuitry (page 5 lines 6-9). The bottom principal surface (50) of the chip carrier (14) is in direct contact with the printed circuit board (page 5 lines 9-18).

The invention of **claim 39** is directed to a light emitting package comprising: a chip carrier (14) having top and bottom principal surfaces (26, 50) (page 3 lines 16-22;

page 4 lines 14-15); at least one light emitting chip (12) attached to the top principal surface (26) of the chip carrier (page 3 lines 16-22); and a lead frame (40, 42) attached to the top principal surface (26) of the chip carrier (page 4 lines 7-12), the lead frame (40, 42) including electrical leads (46, 52) extending from portions of the lead frame attached to the top principal surface (26) of the chip carrier (page 4 lines 12-18), the electrical leads (46, 52) being shaped to include lead portions extended away from the chip carrier (14) that are approximately coplanar with the bottom principal surface (50) of the chip carrier (page 4 lines 12-18).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are pending in this case:

Whether claims 1-6, 15-26, 28-31, and 38-41 are properly rejected under 35 U.S.C. § 103(a) as unpatentable over Peterson et al., U.S. Pat. No. 6,674,159 (hereinafter "Peterson") in view of Kropp, U.S. Pub. No. 2004/0136658 (hereinafter "Kropp").

Whether claim 27 is properly rejected under 35 U.S.C. § 103(a) as unpatentable over Peterson in view of Kropp in further view of Cunningham et al., U.S. Pat. No. 6,005,262 (hereinafter "Cunningham").

VII. ARGUMENT

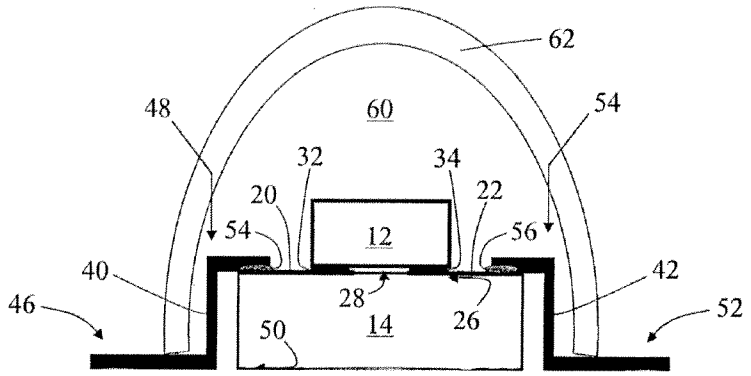
A. The illustrative elected embodiment.

The present application is set forth in the context of the following *background*:

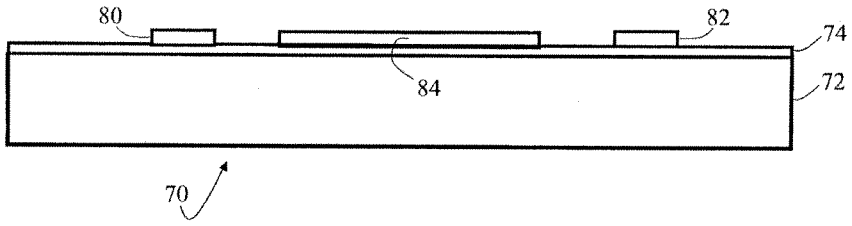
> Surface mounted light emitting packages typically employ a light emitting chip such as a light emitting diode chip ... bonded to a thermally conductive sub-mount which is in turn bonded to a lead frame. The sub-mount provides various benefits such as improving manufacturability of electrical interconnections, improving thermal contact and conduction, and the like. The lead frame is adapted to be surface mounted by soldering to a printed circuit board or other support.
>
> *Such arrangements have certain disadvantages*. The thermal transfer path includes two intervening elements, namely the sub-mount and the lead frame. Moreover, electrical connections to the lead frame typically involve wire bonds, which can be fragile. The mechanical connection between the sub-mount and the lead frame is typically effected in part by an epoxy or other type of encapsulating overmolding material. Such materials can have relatively high coefficients of thermal expansion which can stress wire bonds or mechanical connections.

Present application page 1 lines 9-24 (italics added).

The light emitting packages claimed in the present application address these disadvantages. For illustrative purposes, the elected embodiment of FIGURE 1 of the present application is described. A surface mountable unit includes a chip carrier (14) having top and bottom principal surfaces (26, 50) with a light emitting chip (12) attached to the top principal surface (26) and a lead frame (40, 42) attached to the top principal surface (26) but not to the bottom principal surface (adapted from claim 1):



This package is a surface mountable unit that can be mounted on a printed circuit board (70) on which printed circuitry (80, 82) is disposed:



The surface mountable unit is mounted on the printed circuitry (80, 82) of the circuit board (70) with the lead portions approximately coplanar with the bottom principal surface (50) of the chip carrier (14) electrically contacting the printed circuitry, and the

bottom principal surface (50) of the chip carrier (14) in direct contact with the printed circuit board (adapted from claim 21) to yield the structure shown in FIGURE 1:

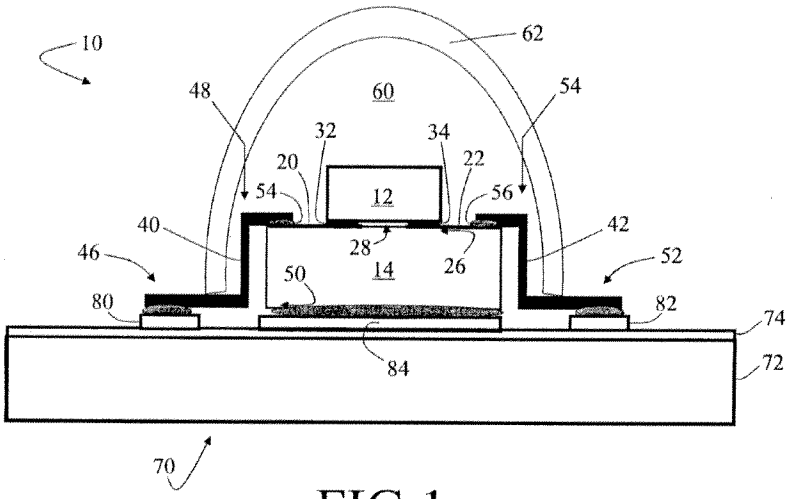


FIG 1

The thermal transfer path includes *only one* intervening element, namely the chip carrier (14), but does *not* include the lead frame (40, 42). Electrical connection of the surface mount package to the circuit board does not employ fragile wire bonds, but instead can employ direct soldering or similar techniques. This is achieved *without* interposing the lead frame between the chip carrier and the circuit board because the electrical leads (46, 52) are shaped to include lead portions approximately coplanar with the bottom principal surface (50) of the chip carrier (14), *see e.g.* claim 17).

B. Claims 1-6, 15-26, 28-31, and 38-41 patentably distinguish over the proposed combination of Peterson and Kropp.

Claim 1 recites a light emitting package comprising: a chip carrier having top and bottom principal surfaces; at least one light emitting chip attached to the top principal surface of the chip carrier; and a lead frame attached to the top principal surface of the chip carrier but not to the bottom principal surface of the chip carrier.

In applying the proposed combination of Peterson and Kropp against claim 1, the Office Action mailed December 28, 2010 (hereinafter "Office Action" or "Final Office Action") identifies the insulating plate (16) of Peterson Figs. 11-12 or 14, or alternatively the monolithic multilayered electrically insulating body (81) of Peterson Figs. 18-19, as the chip carrier, and identifies the microelectronic device (100) as the light emitting chip. Office Action page 3. The lead frame is identified in the Office Action as metallized traces or conductors (24).

However, these electrical traces or conductors (24) do not comprise a lead frame. They are neither a *lead* extending from the package nor a *frame*, that is, a self-supporting element. To the contrary, the skilled artisan would readily recognize the electrical conductors (24) as a *metallized traces* formed on the insulating plate (16), and indeed Peterson repeatedly uses the term "metallized traces" in referring to elements (24). *E.g.*, Peterson col. 9 lines 9, 41, 51, and 61.

Peterson *does* disclose an "electrical lead" as follows:

> Package 8 can also include an *electrical lead 40* attached to assembly 10 at exterior interconnect location 14. Lead 40 can be electrically connected to metallized trace 24. Optionally, lead 40 can be attached to bond pad 28. Peterson col. 9 lines 62-65.

As seen in Fig. 3A, however, the electrical lead (40) is attached to a side of the package, not to the top of the insulating plate or body (16, 81). *See also* lead (88) (Peterson Fig. 5; col. 15 line 46); electrical leads (88, 89) (Peterson Fig. 15B-18; col. 26 line 14). All these electrical leads are attached to the *side* of the package.

The Office Action also cites Kropp as disclosing "lead frame" (51, 52) connecting with the top principal surface of a substrate (3) on which an emission device (1) is mounted. Office Action page 3. However, Kropp does not identify elements (51, 52) as a lead frame, but rather as *wire bonds*. *E.g.*, Kropp ¶[0051] ("electrical contact is made with the laser diode 1 from the topside by means of two bonding wires 51, 52, which lead to contact pads 7 on the printed circuit board 7).

Wire bonds, and the corresponding manufacturing process of "wirebonding", are very well known in the art. For example, a wire bond is illustrated in Peterson Fig. 2, and Peterson explains that "The device or chip is die-attached face-up to a ceramic package and then *wirebonded* to interconnect inside of the package." Peterson col. 2 lines 15-17. Peterson explains that wire bonds use "very thin wires" which are fragile, and the wirebonding process uses a wirebond toolhead. *See* Peterson col. 2 lines 23-32. The present application also mentions wire bonds, and their fragility, at page 1 lines 19-20.

The skilled artisan would not confuse a fragile wire bond with a lead frame. Nor would the skilled artisan consider a wire bond to be an equivalent of a lead frame.

Indeed, the skilled artisan would recognize that wire bonds are not part of the device package *at all*, but rather are electrical connectors that are applied between a device package and a circuit board during *installation* of the device package, using a wirebond toolhead as described in Peterson.

In sum, it is respectfully submitted that neither the metallic traces of Peterson nor the wire bonds of Kropp (or Peterson, for that matter) are lead frames. The Peterson/Kropp combination does not fairly suggest the subject matter of claim 1.

Claim 3 depends from claim 1 and recites one or more areas of electrically conductive material disposed on the top principal surface of the chip carrier, the attachment of the lead frame to the top principal surface electrically contacting the one or more areas of electrically conductive material.

In rejecting claim 3, the Office Action cites the metallic traces (24) of Peterson as corresponding to the electrically conductive material of claim 3. Appellants entirely *agree* with this correspondence.

But: It naturally follows that the metallic traces (24) of Peterson cannot *also* be the lead frame of claim 3 that electrically contacts the one or more areas of electrically conductive material.

Claim 17 depends from claim 1 and recites the lead frame has electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, the electrical leads being shaped to include lead portions approximately coplanar with the bottom principal surface of the chip carrier.

In rejecting claim 17, the Office Action articulates: "the lead frame 24 has electrical leads extending from portions of the lead frame attached to the top principal surface of the chip [carrier], the electrical leads being shaped to include lead portions 702 approximately coplanar with the bottom principal surface of the chip carrier, figs. 15C, 19." Office Action page 5.

Peterson does not refer to elements (700, 702) as electrical leads – rather, Peterson refers to these elements as conductive *vias* that pass *through* the electrically insulating body (81). *E.g.*, Peterson col. 27 lines 24-26; col. 29 lines 29-30. The skilled artisan would not consider these *vias* to be part of a lead frame. The vias (700, 702) are neither a *lead* extending from the package nor a *frame*, that is, a self-supporting structural element.

Claim 38 depends from claim 1 and recites the lead frame includes electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, the electrical leads being shaped to include lead portions distal from the chip carrier that are approximately coplanar with the bottom principal surface of the chip carrier.

In rejecting claim 38 the Office Action merely cites to Peterson Figs. 11D-19. Based on the rejection of claim 17, Appellants guess that the Office is again citing the vias (700, 702) with the chip carrier again being the electrically insulating body (81). But, in addition to the distinctions pointed out with reference to claim 17, the vias (700, 702) are not distal from the chip carrier, whereas claim 38 recites lead portions *distal from* the chip carrier. To the contrary, the vias are *embedded in* the body (81).

Claim 21 is directed to a light emitting package. A chip carrier has top and bottom principal surfaces. At least one light emitting chip is attached to the top principal surface of the chip carrier. A lead frame is attached to the top principal surface of the chip carrier. The lead frame has electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier. The electrical leads are shaped to include lead portions approximately coplanar with the bottom principal surface of the chip carrier. The bottom principal surface of the chip carrier is at least one of substantially electrically non-conductive and electrically isolated from the lead frame, and the chip carrier, light emitting chip, and lead frame define a surface mountable unit. The light emitting package further includes a printed circuit board on which printed circuitry is disposed. The surface mountable unit is mounted on the printed circuitry with the lead portions approximately coplanar with the bottom principal surface of the chip carrier electrically contacting the printed circuitry. The bottom principal surface of the chip carrier is in direct contact with the printed circuit board.

The Office Action again identifies a "lead frame" in Peterson as the combination of the metallic traces (24) and the internal vias (700, 702). It is again respectfully submitted that the skilled artisan would not recognize either of these components as a lead frame. The cited components (24, 700, 702) neither extend away from the chip carrier (as per a "lead") nor define a self-supporting element (as per a "frame").

The Office Action also cites Kropp respective to claim 21, identifying element (1) as an LED, element (4) as a carrier, element (6) as a printed circuit board, and element (51, 52) as a lead frame. Office Action page 6. However, the *wire bonds* (51, 52) of Kropp are not a lead frame and are not an equivalent of a lead frame. Moreover, the

wire bonds (51, 52) do not include a portion that is approximately coplanar with either the substrate (3) or the substrate (4).

Claim 39 recites a light emitting package comprising: a chip carrier having top and bottom principal surfaces; at least one light emitting chip attached to the top principal surface of the chip carrier; and a lead frame attached to the top principal surface of the chip carrier, the lead frame including electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, the electrical leads being shaped to include lead portions extended away from the chip carrier that are approximately coplanar with the bottom principal surface of the chip carrier.

In rejecting claim 39 the Office Action again cites to Peterson elements (24, 700, 702). However, none of those elements comprise electrical leads being shaped to include lead portions *extended away from the chip carrier* that are approximately coplanar with the bottom principal surface of the chip carrier. The metallic traces (24) lie on the top surface of the electrically insulating body (81), and the vias (700, 702) pass *through* the electrically insulating body (81).

The Office Action also cites Kropp respective to claim 39, again identifying element (1) as an LED, element (4) as a carrier, element (6) as a printed circuit board, and element (51, 52) as a lead frame. Office Action page 9. However, the *wire bonds* (51, 52) of Kropp are not a lead frame and are not an equivalent of a lead frame. Moreover, the wire bonds (51, 52) do not include a portion that is approximately coplanar with either the substrate (3) or the substrate (4).

C. Claim 27 patentably distinguishes over the proposed combination of Peterson, Kropp, and Cunningham.

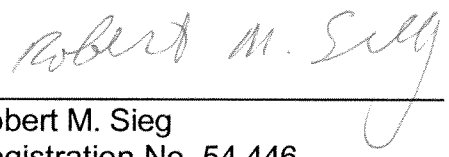
Claim 27 depends from claim 1 and recites the chip carrier comprises electrically conductive silicon having at least the top principal surface coated with an insulating layer. The Office Action cites Cunningham as allegedly showing this feature.

Cunningham is not cited as remedying any of the deficiencies of base claim 1 set forth in Section B herein. Accordingly, Appellants respectfully submit that claim 27 patentably distinguishes over the proposed combination of Peterson, Kropp, and Cunningham at least because base claim 1 distinguishes patentably over this combination of references.

CONCLUSION

For all of the reasons discussed above, it is respectfully submitted that the rejections are in error and that all pending claims 1-6, 15-31, and 38-41 are in condition for allowance. For all of the above reasons, Appellants respectfully request this Honorable Board to reverse the all pending rejections of the appealed claims.

Respectfully submitted,



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APPENDICES

VIII. CLAIMS APPENDIX

Claims involved in the Appeal are as follows:

1. A light emitting package comprising:

a chip carrier having top and bottom principal surfaces;

at least one light emitting chip attached to the top principal surface of the chip carrier; and

a lead frame attached to the top principal surface of the chip carrier but not to the bottom principal surface of the chip carrier.

2. The light emitting package as set forth in claim **1**, further comprising:

an encapsulant encapsulating at least the light emitting chip and the top principal surface of the chip carrier, the bottom principal surface of the chip carrier and leads of the lead frame extending outside the encapsulant.

3. The light emitting package as set forth in claim **1**, further comprising:

one or more areas of electrically conductive material disposed on the top principal surface of the chip carrier, the attachment of the lead frame to the top principal surface electrically contacting the one or more areas of electrically conductive material.

4. The light emitting package as set forth in claim **3**, wherein the one or more areas of electrically conductive material include:

a first area of electrically conductive material defining a first electrical terminal;

a second area of electrically conductive material electrically isolated from the first area, the second area defining a second electrical terminal of opposite electrical polarity from the first electrical terminal;

electrodes of the light emitting chip being electrically connected with the first and second electrical terminals; and

the lead frame being attached to the first and second electrical terminals.

5. The light emitting package as set forth in claim **4**, wherein the light emitting chip is flip-chip bonded to the first and second electrical terminals.

6. The light emitting package as set forth in claim **4**, wherein the light emitting chip is flip-chip bonded to the first and second electrical terminals using one of thermosonic bonding, solder, and a conductive epoxy.

7-14. (Withdrawn)

8. The light emitting package as set forth in claim **7**, wherein another electrode of the light emitting chip is wire bonded to the other one of the first and second electrical terminals.

9. The light emitting package as set forth in claim **3**, wherein:

the one or more areas of electrically conductive material include:

a first area of electrically conductive material defining a first electrical terminal,

a second area of electrically conductive material electrically isolated from the first area, the second area defining a second electrical terminal of opposite electrical polarity from the first electrical terminal, and

a third area of electrically conductive material electrically isolated from the first and second areas of electrically conductive material, the third area of electrically conductive material defining a series interconnection terminal; and

the light emitting chip includes first and second light emitting chips, electrodes of the first light emitting chip being electrically connected with the first and series interconnection electrical terminals and electrodes of the second light emitting chip being electrically connected with the second and series interconnection electrical terminals, and the lead frame being attached to the first and second electrical terminals.

10. The light emitting package as set forth in claim **9**, wherein the light emitting chip further includes:

a third light emitting chip, electrodes of the third light emitting chip being electrically connected with the first and series interconnection electrical terminals.

11. The light emitting package as set forth in claim **10**, wherein the light emitting chip further includes:

a fourth light emitting chip, electrodes of the fourth light emitting chip being electrically connected with the second and series interconnection electrical terminals.

12. The light emitting package as set forth in claim **9**, further including:

at least one zener diode electrically connected with at least one of

the first and series interconnection electrical terminals, and

the second and series interconnection electrical terminals.

13. The light emitting package as set forth in claim **3**, further including:

at least one electronic component electrically contacting the one or more areas of electrically conductive material, the at least one electronic component regulating behavior of the at least one light emitting chip.

14. The light emitting package as set forth in claim **13**, wherein the at least one electronic component includes:

a zener diode electrically connected in parallel with the light emitting chip to provide electrostatic discharge protection.

15. The light emitting package as set forth in claim **1**, wherein the light emitting chip receives electrical power through the lead frame and does not receive electrical power through the bottom principal surface of the chip carrier.

16. The light emitting package as set forth in claim **1**, wherein the bottom principal surface of the chip carrier is electrically isolated from the lead frame.

17. The light emitting package as set forth in claim **1**, wherein the lead frame has electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, the electrical leads being shaped to include lead portions approximately coplanar with the bottom principal surface of the chip carrier.

18. The light emitting as set forth in claim **17**, wherein the bottom principal surface of the chip carrier is at least one of substantially electrically non-conductive and electrically isolated from the lead frame.

19. The light emitting package as set forth in claim **18**, wherein the chip carrier, light emitting chip, and lead frame define a surface mountable unit, the light emitting package further comprising:

printed circuitry, the surface mountable unit being mounted on the printed circuitry with the lead portions approximately coplanar with the bottom principal surface of the chip carrier electrically contacting the printed circuitry.

20. The light emitting package as set forth in claim **19**, further comprising:

a printed circuit board including the printed circuitry, the bottom principal surface of the chip carrier being in thermal contact with the printed circuit board.

21. A light emitting package comprising:

a chip carrier having top and bottom principal surfaces;

at least one light emitting chip attached to the top principal surface of the chip carrier;

a lead frame attached to the top principal surface of the chip carrier, the lead frame having electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, the electrical leads being shaped to include lead portions approximately coplanar with the bottom principal surface of the chip carrier;

wherein the bottom principal surface of the chip carrier is at least one of substantially electrically non-conductive and electrically isolated from the lead frame and the chip carrier, light emitting chip, and lead frame define a surface mountable unit;

a printed circuit board on which the printed circuitry is disposed, the surface mountable unit being mounted on the printed circuitry with the lead portions approximately coplanar with the bottom principal surface of the chip carrier electrically contacting the printed circuitry, the bottom principal surface of the chip carrier being in direct contact with the printed circuit board.

22. The light emitting package as set forth in claim **21**, wherein the chip carrier is soldered to the printed circuit board.

23. The light emitting package as set forth in claim **21**, wherein the chip carrier is soldered to the printed circuit board, said soldered connection being thermally conductive but not conducting electrical current when the light emitting chip is operated.

24. The light emitting package as set forth in claim **21**, wherein an attachment between the lead portions contacting the printed circuitry is different from an attachment of the bottom principal surface of the chip carrier contacting the printed circuit board.

25. The light emitting package as set forth in claim **21**, further comprising:

an encapsulant encapsulating at least the light emitting chip and the top principal surface of the chip carrier, the bottom principal surface of the chip carrier and at least the lead portions approximately coplanar with the bottom principal surface of the chip carrier extending outside the encapsulant.

26. The light emitting package as set forth in claim **1**, wherein the chip carrier comprises:

a semi-insulating silicon wafer.

27. The light emitting package as set forth in claim **1**, wherein the chip carrier comprises:

electrically conductive silicon having at least the top principal surface coated with an insulating layer.

28. The light emitting package as set forth in claim **1**, wherein the chip carrier comprises:

metal having at least the top principal surface coated with an insulating layer.

29. The light emitting package as set forth in claim **1**, wherein the chip carrier comprises:

thermally conductive plastic.

30. The light emitting package as set forth in claim **1**, wherein the chip carrier comprises:

ceramic.

31. The light emitting package as set forth in claim **1**, wherein the chip carrier is electrically insulating and the lead frame is electrically conductive.

32-37. (Canceled)

38. The light emitting package as set forth in claim **1**, wherein the lead frame includes electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, the electrical leads being shaped to include lead portions distal from the chip carrier that are approximately coplanar with the bottom principal surface of the chip carrier.

39. A light emitting package comprising:

a chip carrier having top and bottom principal surfaces;

at least one light emitting chip attached to the top principal surface of the chip carrier; and

a lead frame attached to the top principal surface of the chip carrier, the lead frame including electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, the electrical leads being shaped to include lead portions extended away from the chip carrier that are approximately coplanar with the bottom principal surface of the chip carrier.

40. The light emitting package as set forth in claim **1**, further comprising:

solder bonds attaching the lead frame to the top principal surface of the chip carrier.

41. The light emitting package as set forth in claim **39**, further comprising:

solder bonds attaching the lead frame to the top principal surface of the chip carrier.

IX. EVIDENCE APPENDIX

NONE

X. RELATED PROCEEDINGS APPENDIX

NONE